IC Compiler

Comprehensive Place and Route System

Overview

IC Compiler is the leading place and route system. A single, convergent, chip-level physical implementation tool, it includes flat and hierarchical design planning, placement, clock tree synthesis, routing and optimization, manufacturability, and low-power capabilities that enable on schedule delivery of advanced designs at all process nodes.

- IC Compiler is the industry leading place-and-route system for established and emerging process technology node designs.
- Multicore support throughout the flow delivers improved productivity. New technologies, like concurrent clock and data (CCD) with clock concurrent optimization, PrimeTime physically-aware engineering change order (PT-ECO) guidance with minimum physical impact implementation, and golden unified power format (IEEE 1801 UPF), enable designers to handle gigascale design complexity and meet tight project schedules.
- IC Compiler hierarchical design technology enables powerful design planning and early chip level exploration / analysis features to handle large, complex designs.
- IC Compiler delivers smaller die size with predictable design closure to reduce the cost of design.
- IC Compiler with Zroute digital router technology utilizes advanced routing algorithms, concurrent manufacturability optimizations and multi-threading, to improve manufacturability and deliver faster turn-around-time.
- IC Compiler In-Design technology seamlessly integrates the IC Validator signoff DRC and metal fill solution allowing designers to mitigate manufacturing compliance challenges in the implementation stage for faster signoff closure.
- IC Compiler is the cornerstone of the Galaxy™ Design Platform and is tightly correlated to the industry-standard signoff solutions – PrimeTime® SI and StarRC™ with value links to Design Compiler® Graphical.

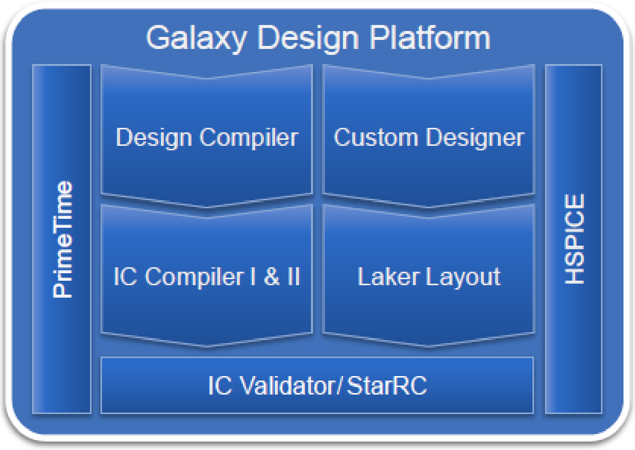

Figure 1: Synopsys Galaxy Design Platform

Benefits

IC Compiler delivers all the technology required to realize both mainstream and advanced designs at any process node, from the established nodes still in use (e.g., 0.35µm, 0.25µm, 180nm, 130nm, 90nm, 65nm, 45nm) to the latest emerging process nodes at 20nm and below. IC Compiler is the leading physical implementation tool and is uniquely positioned with value links to Design Compiler Graphical®, PrimeTime SI, StarRC, IC Validator, Custom Designer, the Galaxy Custom Router, and PrimeRail. Beyond value links, IC Compiler shares technology with and correlates to Design Compiler Graphical, PrimeTime SI and StarRC to ensure a fast and monotonic path from design to final signoff. Additionally, IC Compiler In-Design technology enables early physical verification and fixing using IC Validator technology and accurate foundry runsets.

IC Compiler benefits the physical designer in four key categories: Quality of Results, Turn-around Time, Ease of Use, and Cost of Design.

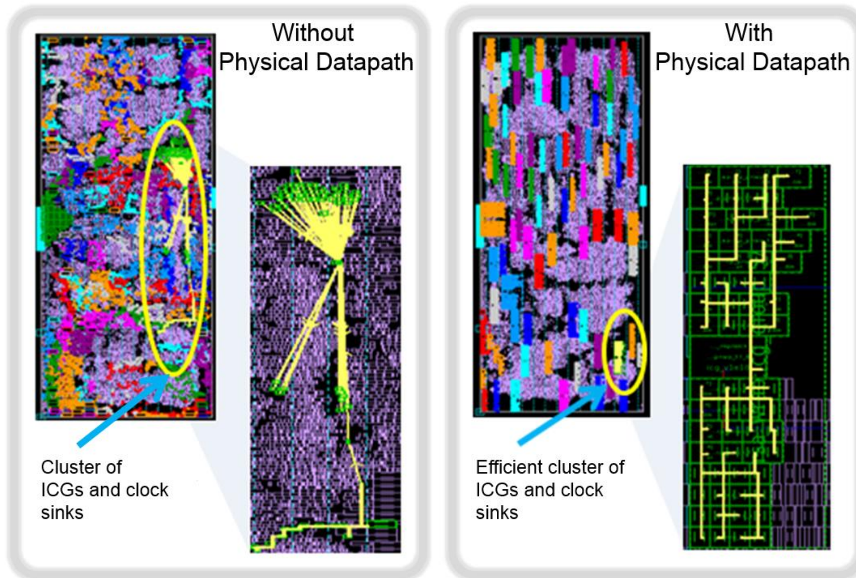

Figure 2: Physical datapath reduces power and improves routability

Quality of Results

Innovative multicorner multimode (MCMM) and multivoltage (MV) technologies in IC Compiler digital implementation system delivers improved QoR, measured in terms of the complete cost vector – timing, area, power, signal integrity, routability, robustness and manufacturability.

- **Physical datapath**: Physical datapath technology allows designers to create regular placement structures by specifying constraints for the relative row and column positions of cell instances. Figure 2 highlights some of the benefits of physical datapath. User controlled data element array packing leads to better timing and routing predictability. By using physical datapath designers also lower power and reduce die area.

- **TIO**: Transparent interface optimization (TIO) targets concurrent optimization with full path visibility at both the top and block interface levels. Since the entire path is considered, TIO achieves monotonic progress towards design closure in extremely large abutted or nearly abutted designs. Moreover, automatic block updates may be multi-core processed and distributed to realize even more timing closure acceleration.

- **CCD**: Concurrent clock and data (CCD) clock concurrent optimization technology delivers the highest QOR for advanced designs and complex clocking architectures. CCD technology is a key enabler for high-speed processors and SOCs. The categorized timing report shown in figure 3 greatly accelerates clock timing analysis and debug. The categorized timing report is cross-linked to the layout to facilitate problem resolution.

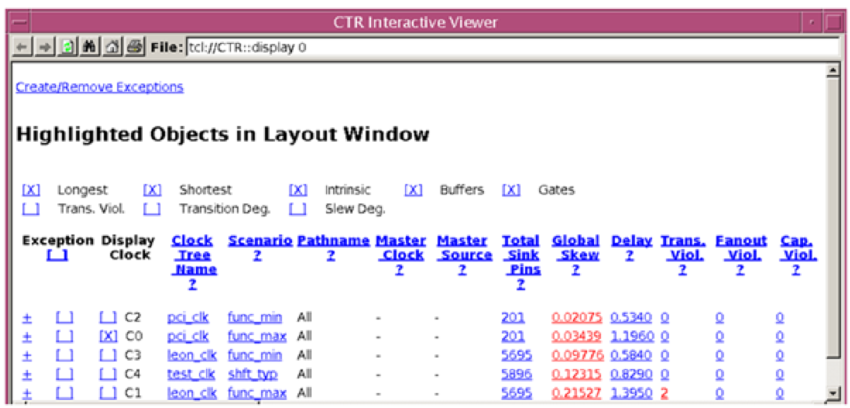

Figure 3: Categorized timing report

- **Mesh technologies:** IC Compiler CTS offers the most comprehensive automatic mesh solutions in the industry. Pure clock mesh offers the best timing and variation tolerance performance, while multisource CTS, a hybrid mesh approach, balances the ease and low power benefits of conventional CTS with the frequency and robustness of pure clock mesh.

- **ARM cores:** IC Compiler is the preferred solution used on the majority of high performance ARM core tapeouts. Performance, power and area (PPA) targets are met with a wide arsenal of key technologies that may be applied, such as: clock mesh, CCD, physical datapath, hierarchical design planning, multi-power domains, route-based optimizations, MCMM, Zroute, UPF and minimum physical impact (MPI) ECO.

Turn-around Time

IC Compiler provides the fastest path to results. This is achieved using best in-class engines, multicore support, powerful design planning capabilities, and complete, faster convergence throughout the design stages, culminating in unrivalled signoff accuracy.

- **Data flow analysis**: Data flow analysis (DFA) during design planning enables fast and optimum block placement in large block dominated designs. Data flow visibility allows the designer to minimize path lengths through block array design and orientation, speed up design planning, and improve timing budget quality. Figure 4 shows an example of connectivity visualization using data flow analysis.

- **MPI-ECO**: Minimum physical impact (MPI) technology reduces tapeout delays due to late stage ECOs. MCMM and multivoltage-aware MPI leverages PrimeTime signoff ECO guidance to place ECO cells with minimum disturbance to the existing layout and to re-use as much of the existing route segments as possible, resulting in faster, more accurate ECOs and better turn-around time.

- **Zroute:** Zroute technology digital router technology in IC Compiler utilizes advanced digital routing algorithms and multi-threading capability to take full advantage of the multi-core compute platforms delivering much faster turn-around time. The modern Zroute architecture incorporates state-of-the-art routing technology, such as native soft rules to enable litho-friendly routing and avoid manufacturing problems. Employing concurrent manufacturability optimization techniques, Zroute simultaneously considers the impact of manufacturing rules, redundant vias, timing and other design goals to deliver the highest QoR along with improved manufacturability.

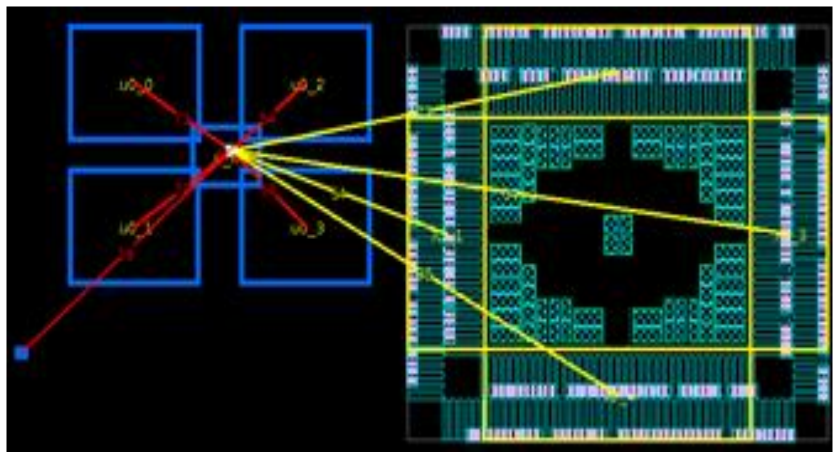

Figure 4: Data flow analysis visualizes design connectivity

Ease of Use

IC Compiler advances ease-of-use with intuitive commands to deliver best out-of-the-box results.

- **GUI visualization**: The IC Compiler GUI provides user friendly and easy-to-use features that enable designers to resolve issues at all design stages. The GUI enables fast analysis, visualization, debugging and repair features. The powerful error browser simplifies and accelerates manual intervention for the last few remaining DRCs.

- **Lynx:** The Lynx Design System is a separate product that is widely leveraged by IC Compiler users giving designers access to a production proven flow right out-of-the-box. Lynx users can customize the design flow to the targeted technology node for each specific design, from established nodes to the latest emerging nodes. Lynx provides flow customization decision assistance and a cockpit that provides both flow metrics as well as project visualization. Lynx lowers flow development and maintenance cost, freeing resources to generate true product differentiation.

- **Golden UPF**: UPF handling is simplified for Design Compiler and IC Compiler. The Golden UPF file remains unchanged throughout the flow. Automated name change handling minimizes UPF side file requirements.

- **3DIC and flip chip router:** Redesigned 45 degree flip chip router enables RDL bump, interposer, and chip finishing routing within the IC Compiler environment.

Cost of design

IC Compiler allows designers to utilize a variety of techniques to meet timing, power, area, routability, and yield goals. This reduces the cost of design and increases predictability.

- **Correlation, consistency checker and enabler:** IC Compiler timing results correlate closely to PrimeTime. A consistency checker is provided to report differences in settings and an enabler corrects and resets both PrimeTime and IC Compiler environments to the recommended settings to produce best correlation.

- **MCMM:** Concurrent MCMM-aware placement, clock tree synthesis, routing, and optimization transformations dramatically reduce TAT for large, complex chips with multiple numbers of modes and corners. Intelligent optimization is driven by timing, area, power, signal integrity, routability and yield cost factors that are measured concurrently across all scenarios. IC Compiler's MCMM solution eliminates the ping-pong effects typically seen at later stages of the design flow.

- **Manufacturing awareness**: IC Compiler offers the only complete solution available to optimize for yield and manufacturability. Concurrent manufacturability optimizations reduce the number of remaining single vias, and the critical area for higher yield while still meeting timing QoR.

- **Design for test**: IC Compiler as part of the Synopsys Galaxy Implementation Platform provides a comprehensive test automation solution that offers system-on-chip designers the fastest and most cost-effective path to high quality manufacturing tests and working silicon. IC Compiler performs physically-aware timing-driven scan chain re-partitioning and reordering. Fully-integrated DFT MAX™ test compression and synthesis technology achieves high compression without affecting the test coverage, functionality, timing, or power requirements of the design.

- **20nm and below enablement:** IC Compiler adds 20nm and 16nm support for emerging process technology through the IC Compiler AG package.

  - **Double patterning and beyond**: Double patterning (DPT) or multiple-patterning starting at 20nm and below designs requires at least two masks to correctly manufacture integrated circuits with current lithography equipment. Synopsys TCAD technology participates in the bring-up of new process nodes and the early knowledge leads to the fast maturation of IC Compiler technology for the emerging advanced nodes. IC Compiler produces DPT clean layouts. Additionally, IC Compiler and In-Design physical verification with IC Validator offers an accelerated multi-patterning closure solution.

  - **Emerging rule support**: The earliest and most complete emerging process rule support is ensured by foundry use of IC Compiler with Zroute digital router technology to develop the new processes. Innovative soft rule support allows rule relaxation in non-critical situations to enable even the most challenging designs to achieve fast and efficient routing closure.

  - **FinFET support**: Complete FinFET support is another benefit of the early co-development collaboration between Synopsys and the leading foundries. IC Compiler fully supports FinFET use through all physical design stages.

Features

- Multicore support for higher throughput for designs in established silicon technologies
- High performance for emerging silicon technologies
- Comprehensive optimization capabilities meet timing, area, power, signal integrity, routability and manufacturing objectives
- Predictability during the implementation process
- Single timer
- Complete netlist-to-GDSII solution for best QoR and TTR

QoR

- Common engines throughout the flow
- Single timer
- Innovative optimization capabilities in timing, area, DFT, power, routability and manufacturability ensure best QoR
- Layer aware optimization
- Multisource CTS delivers better skew, and reduces OCV and power
- Robust clock mesh technology for very tight skew control
- Physical datapath delivers better QoR and predictability for effective datapath management in high speed designs
- Clock mesh support to handle clock variations at advanced nodes

TAT

- Concurrent MCMM optimization throughout the implementation flow

- Tight correlation with Design Compiler Graphical through Synopsys physical guidance (SPG)
- Physical datapath enables dramatic improvement in productivity for structured logic, ICG and cluster implementation and provides predictable results in timing, area, and power
- Faster top level closure with Transparent Interface Optimization
- Robust crosstalk flow during all stages; detects and fixes crosstalk violations
- Faster ECO flow with intelligent MCMM, MV aware PrimeTime-SI guidance for faster signoff
- Faster ECO flow with physically-aware ECO guidance and minimum physical impact (MPI)

Low Power

- Supports Unified Power Format (IEEE 1801 UPF standard) throughout the flow
- Support for multi-voltage designs during design planning, synthesis, placement, clock tree synthesis, routing, chip finishing and ECO stages
- Advanced algorithms deliver high-quality dynamic and leakage optimization results
- Power-aware placement technology groups registers to reduce dynamic power
- Support for complex clock gating in clock tree synthesis
- Low-power, SI-aware CTS
- Signal electromigration analysis and repair significantly improves design reliability
- In-Design static rail and EM analysis with PrimeRail and IC Compiler improves designer productivity

Signoff

- Highly correlated with golden signoff solutions: PrimeTime SI and StarRC
- Shares common infrastructure and technologies with PrimeTime, such as Arnoldi, OCV, CRPR, CCS, common cell delay calculation and SDC constraints to ensure tight correlation
- Advanced On-Chip Variation (AOCV) support for clock and data improves TTR and eliminates extra margins
- Parametric On-Chip Variation (POCV) support to reduce graph based to path based pessimism.
- In-Design physical verification with IC Validator and IC Compiler help achieve optimal metal fill and signoff quality DRC checking in the design stage

Ease of Use

- Tcl support throughout
- Advanced route editing features

GUI

- Powerful features enable design analysis, visualization, debugging, and fixing
- Cross-referencing between logic vs. physical analysis
- Clock tree synthesis skew and latency analysis
- Hierarchical clock tree browser
- Power Network Analysis (PNA)
- Visual maps for worst negative slack (WNS)/congestion/cell density/scan/ leakage power/dynamic power/total power and more
- Critical area analysis (CAA)
- Fast physical data analysis and editing

Manufacturing Awareness

- Complete support for advanced design rules
- Soft rule support
- Critical Area Analysis (CAA)
- Optimization of critical areas through wire-spreading/widening during global route, track assignment and detailed routing
- Automated, timing driven multipattern via selection
- Staggered metal fill
- Litho-friendly routing
- Faster In-design flow with IC Validator physical verification technology for accurate metal fill and automated DRC fixing

Design Planning

- Concurrent hierarchical design
- Complete design planning solution for hierarchical and flat designs
- Early analysis and feasibility exploration capabilities
- Multi-million instance design capacity
- Complete multi-voltage flow with MTCMOS support
- Power network analysis (PNA), Power network synthesis (PNS), and power pad synthesis capabilities
- Easier handling of complex P/G structures using template-based PNS
- Timing-driven automatic macro placement
- Improved floorplans with Data Flow Analyzer (DFA) capability
- Full Flip Chip design flow support

DFT

- Physically partitioned and optimized scan chains deliver predictable timing closure
- Physical test-optimized flow with support for DFT Compiler and DFT MAX features using scanDEF interface

Interfaces

Library Interface

- Reads LIB synthesis library containing functionality, timing, and design rule constraints
- Reads Milkyway (MWY) physical library describing technology and cell outlines
- Reads LEF through Milkyway data prep, technology file (TF) format

Inputs

- Verilog netlist
- SDC, DEF, SPEF, SBPF, ALF, TLUPlus
- Several user-level commands are provided for specifying and modifying the floorplan

Outputs

- Verilog netlist
- SDC, DEF, SPEF, SBPF
- GDSII
- OASIS

User Interfaces

- Tcl or GUI-based user interface
- All Design Compiler reports enhanced with physical information; additional reports and commands enable analyzing layout and checking consistency of libraries and input files

Platform Support

IC Compiler supports major hardware platforms

IC Compiler is the most complete and comprehensive physical implementation solution available. For detailed information regarding a specific technology need, please contact your local Synopsys account team or visit www.synopsys.com.