Laker³ Custom Design Tools

The Laker³™ Custom Design Tools form a unified front-to-back environment for custom circuit design and layout. They deliver a complete solution for analog, mixed-signal, and custom digital design and layout that is optimized for performance and interoperability for 28-nanometer (nm) and below design flows.

Widely-used Interoperable Custom Design Flow

Based on the industry standard OpenAccess (OA) database, and with full support for interoperable process design kits (iPDKs), the Laker³ is the latest generation of the widely-used interoperable custom design flow. Laker³ is the mainstream custom design solution at leading fabless semiconductor companies, merchant foundries and integrated device manufacturers.

Laker³ provides unparalleled interoperability and an open environment that enables companies to incorporate best-in-class third-party tools for analog simulation, physical verification, extraction and much more. This open system provides:

- Compatibility with legacy design tools—view/edit schematics or layouts created with other OA-based tools
- Integration with leading signoff tools for real-time design rule checking during layout editing
- Complete support for parameterized devices written in open standard languages, such as Python, Tcl or C++

Laker³ Infrastructure

Figure 1: The Laker³ product family
Laker® tools are anchored by a performance-driven infrastructure with ultra-fast drawing capabilities, and 2-10X faster read/write operations compared to other custom design tools. The unified binary executable of Laker® combines design entry, custom layout, custom digital place-and-route, and analog prototyping tools into a single environment. This enables passing of design intent between tools and makes it easy to communicate design changes. Laker® employs a modern graphical user interface (GUI) based on QT with modern features, such as tabbed windows, one-click open for recently closed designs, and configurable tools.

**Laker® Tools**
The Laker® solution includes tools for design entry, analysis, and layout including:
- Laker Advanced Design Platform
- Laker Custom Layout System
- Laker Custom Digital Placer and Router
- Laker Analog Prototyping Tool

**Laker Advanced Design Platform**
The Laker Advanced Design Platform (ADP) integrates the full-featured Laker schematic editor, open simulation console and waveform analyzer into a single circuit design environment. It provides integration of most analog simulators to supply a complete solution for the design of analog, mixed-signal, RF, memory, and custom digital IC designs.

**Laker Custom Layout System**
The Laker Custom Layout System provides rule-driven and schematic-driven layout features for generating full-custom layouts in a much shorter time than manual layout methods. Its controllable automation technology simplifies the layout process while reducing verification and debug efforts.

**Laker Custom Row Placer and Router**
The Laker Custom Row Placer and Router tools are ideal for automating the placement and routing of cell-based custom digital blocks that are ordinarily created by hand. Together, they facilitate rapid creation of hand-crafted quality digital blocks for mixed-signal, memory, and custom digital integrated circuits.

**Laker Analog Prototyping Tool**
The Laker Analog Prototyping tool automates the placement of analog devices. This improves layout productivity and provides designers with fast feedback of layout-dependent effects. It has built-in understanding of analog layout requirements, so it is much easier to adopt and deploy than competing analog automation tools.

**Laker Custom Layout Automation System**
The Laker Custom Layout Automation System offers powerful solutions for analog, mixed-signal, memory, and custom digital IC design that address key challenges in the layout process. Hundreds of companies have deployed the Laker Custom Layout System in their design flows to produce high-quality, high-density layout of advanced chip designs. The Laker layout system provides an intuitive methodology and controllable automation for efficiently achieving superior layout results. The Laker layout system helps
- Automate many tedious and error-prone layout tasks
- Minimize CAD support requirements
- Reduce overall cost of design

**Core Features**
The Laker layout system provides rule-driven layout so users can rapidly realize, place, route, and edit physical layout that is DRC- and LVS-correct. Unique controllable automation simplifies numerous tasks from measurement to device generation. The built-in DRC engine drives the application of design rules through device generation, layout, and routing.

**MCells**
In addition to supporting interoperable iPDK devices, Laker also has built-in “MCell” parameterized device technology. MCells enable a highly automated schematic-driven layout (SDL) flow that includes the user-controllable device planning, wiring and manipulation capabilities of the Stick Diagram Compiler.
- MCells include transistors, resistors, capacitors, contacts/vias and guardrings

![Figure 2: Schematic-driven layout in the Laker® environment](image)
MCells enable the rapid generation of optimized layout structures for complex devices, such as multiple-gate transistors, guardrings, contact arrays, interdigitized resistors and capacitors.

Rule-driven layout
Laker automatically checks, displays, and snaps to width, space, notch, overlap, and enclosure rules in real-time. With Laker rule-driven layout, users can:
- Ensure LVS-correct layout results with flight lines that display connectivity information to guide and speed-up wiring operations.
- Automatically identify any created shorts in real-time.
- Supports both recommend and DFM rules for width, space, notch, overlap and enclosure.

Built-in Routers
The Laker Custom Layout system’s built-in routers use the design’s connectivity to automatically finish wiring “on-the-fly.” Features include:
- Point-to-point router that lets you either automatically or interactively create a DRC-correct route between the source and target.
- Interactive, DRC-correct pathfinder that follows the cursor in “point-and-click” routing mode.
- Route-by-label function that automatically creates routes as guided by text or labels.
- Net router that automatically routes single or multiple nets.

Advanced Features
The Laker Custom Layout system uses unique technologies to exploit design rules, connectivity and parameters during layout in an efficient, consistent, and automatic way. The system’s SDL capabilities save you time so you can focus on creating the best possible layout. By handling dozens of critical requirements in an automated yet natural way, the Laker layout system keeps users in complete control of the layout quality.

Schematic-driven layout
Both netlist and schematic views are included with the Laker layout editor for an intuitive SDL working environment. Laker SDL includes full support for hierarchical design. With Laker SDL, schematic hierarchy and layout hierarchy can be manipulated independently. Layout designers can organize the layout hierarchy in the way that works best for them while still being able to cross probe and drag and drop from the schematic.
**Stick Diagram Compiler**

The Stick Diagram Compiler provides users with a way to optimize device layout at a higher level of abstraction. Layout designers can swap, merge, move, split and align gates at a symbolic level without having to worry about design rules, connectivity or parameter values. It includes built-in automatic multi-row transistor placement capability for PMOS and NMOS transistors.

**Laker Advanced Design Platform (ADP)**

The Laker Advanced Design Platform (ADP) integrates the full-featured Laker schematic editor, open simulation console and LakerWave™ waveform analyzer into a single circuit design environment. Laker ADP is based on the OpenAccess standard, and delivers unsurpassed design tool interoperability.

**Schematic Editor**

- Manual and automated symbol generation enables users to quickly create new or higher-level device symbols
- Automatic symbol placement and wire connection quickly converts third-party netlists into human-readable schematics
- Design Hierarchy Browser maintains an up-to-date design hierarchy tree during schematic creation for real-time visualization and cross-probing with schematic
- Dynamic net highlighting and color differentiation between multiple nets across the hierarchy allows users to easily trace schematic data paths
- Pass constraints directly to the Laker layout system for a schematic-driven layout flow, enabling correct-by-design layout, placement and routing
- Advanced features include hierarchical search-and-replace, multi-sheet schematics, hierarchy editor, infix mode editing, and on-screen parameter editing

**Automatic Schematic Generator**

- Automatically create human-readable, hierarchical schematics for editing, ECO, or layout generation from CDL, SPICE, Verilog gate-level, or EDIF 200 netlists
- Import schematic data for smooth and accurate transfer of design intent, attributes and parameters from circuit design to mask design

**Simulation Control Console**

- Common interface lets users directly link to familiar, best-in-class simulators including HSPICE®, Spectre®, Eldo®, ADiT™, SmartSpice, and MSIM®
- Quickly add probe signals to the simulation console using a simple pick-up operation of a net or device in the schematic
- Back-annotate simulation results to schematic, including node voltage, branch current, device operating point and operating region values
- Corner analysis feature simplifies setup of sweep variables, voltages, temperature and model variations to perform PVT simulations

**LakerWave Waveform Analyzer**

- Powerful and interactive waveform analyzer supports both time domain (digital) and frequency domain (analog) for mixed-signal designers
- Pre-selector easily locates data points for accelerated waveform measurement with gravity capability
- Real-time display of X/Y coordinates and the values for multiple measurements allows dynamically displays results as users move the cursor
- FFT capability simplifies analysis of harmonic distortion
- Analog-to-digital and digital-to-analog conversion functions help integrate digital domain and analog domain for mixed-signal analysis
- Schematic-to-waveform cross-probing enables intuitive, real-time analysis

**Laker Analog Prototyping**

Laker™ Analog Prototyping automates the placement of analog devices to improve layout productivity and provide designers with fast feedback of layout-dependent effects. The tool's built-in understanding of analog layout requirements makes it much easier to adopt and deploy than other analog automation tools. As part of the complete Laker Custom Design family, the analog prototyping tool brings together the award-winning Laker schematic-driven layout tool with significant advancements in automation to speed completion of custom analog layout.
**Analog Prototyping Flow**

Analog prototyping in the Laker environment starts with an analog schematic or netlist. Laker Analog Prototyping analyzes your circuit and automatically generates placement constraints that drive the automatic placement engine to create high-quality placement results. The placement engine generates multiple example placements all of which meet the design constraints. From there, users can refine the constraints as needed until reaching the desired placement. With the ability to rapidly complete the placement of analog circuits, you can generate early placement results for circuit designers to use for layout-aware simulation.

**Core Features**

Laker Analog Prototyping combines all of the Laker SDL features with advanced automation capabilities that include:

- Automatic constraint extraction
- Design rule checking engine with advanced-node rule support
- Pattern editor for placement and routing of matched devices
- Automatic constraint-driven placement
- Hierarchical analog prototyping

**Automatic Constraint Extraction**

Generating proper constraints is an important part of the analog prototyping flow. Laker Analog Prototyping automates this process with an automatic constraint extraction engine. This engine identifies devices that have symmetrical current flows and forms them into symmetry groups. It also recognizes common subcircuit types, such as differential pairs, current mirrors, voltage references, etc., and automatically forms them into matching device patterns. In addition, it finds and forms digital logic into transistor chains with properly-aligned gates. The Laker hierarchical constraint browser permits easy review and editing of the constraints in a design. Laker supports the iPL standard iConstraint format.

**Design Rule Checking Engine**

Laker Analog Prototyping includes the full version of the Laker DRC engine with advanced node support. This engine is used by the Laker placement engine to create design-rule correct placements and substantially improve rule-driven layout editing as compared to basic rule-driven editing operations. Any design rule can be checked dynamically during editing, not just the basic width and spacing rules. After a shape is added, any design rule errors
that Laker detects are displayed with fixing guides that illustrate how an error can be corrected. The DRC engine can work directly from the Laker technology file for many of the design rules, so no special rule file is required.

**Pattern Editor for Placement and Routing of Matched Devices**

One of the most powerful productivity-enhancing features in Laker is the matched device creator, a symbolic pattern editor for handling matching devices. Users can draw from the built-in Laker pattern library to apply matching placement patterns to devices, for example, placing a differential pair in a common centroid configuration. The pattern library can be extended with user-generated custom patterns of device placement. Laker Analog Prototyping also features matched device routing capability. With the matched device router, users can automatically generate routing patterns for matched device. If needed, users can modify the routes generated by the matched device router by simply dragging and dropping the wires to a new location. When the pattern is instantiated into the layout, DRC-correct wiring is included.

**Automatic Constraint-driven Placement**

The automatic constraint-driven placement in Laker Analog Prototyping is capable of meeting a variety of analog constraints, including symmetry, matching, cluster, spacing and variation constraints. It generates multiple solutions so users can explore a variety of potential solutions.

The placer uses the built-in LiveDRC design rule checker to generate design-rule-correct placements. It also checks for routability using a built-in trial router and adds space between components as needed to create a routable placement. The placer can also enforce constraints related to layout-dependent effects (LDE). Pin placement can be handled automatically, or it can be taken from the pin locations in the schematic or from a floorplan layout. The floorplan layout can also be used to preplace critical devices. The placer maintains the relative locations of preplaced devices from the floorplan when placing the remaining devices.

**Hierarchical Analog Prototyping**

Hierarchical prototyping is supported with the Laker physical hierarchy manager. The hierarchy manager GUI shows the block present in a design and allows users to configure the constraint extraction and placement settings for each block. During hierarchical placement, multiple potential solutions are generated for sub-block use in the next level in the hierarchy with only the best solutions preserved. This process continues until the top-level hierarchy is reached. With Laker hierarchical analog prototyping, designs with thousands of devices can be placed in just minutes.

**Laker Custom Row Placer**

The Laker Custom Row Placer provides automation for the placement of custom digital cells that would normally be placed by hand. It allows precise custom placement of the digital blocks used in mixed-signal and custom digital designs.
Core Features

- Support for fixed-height standard cell, custom cell, and double-height cell designs
- Stacking utilities for datapath-style placement
- Row snapping and overlap removal during interactive editing
- Congestion-driven placement to minimize wire length
- Automatic and manual addition and removal of filler, well tap, and end cap cells

Laker Custom Digital Router

The Laker Custom Digital Router is ideal for automating the routing of blocks that are normally routed by hand, such as the control logic sections of memory designs. It features:

- Unique hybrid routing technology that combines gridded and shape-based routing for very high route completion rates while being DRC clean.
- Spine routing for memory-style routing with restricted metal layers
- Post-route optimization that includes double-via insertion, antenna fixing and jog removal
- Power and ground grid placement and routing for a complete solution
- LEF/DEF and Verilog import and LEF/DEF export capabilities
- Advanced nanometer rule support

Figure 12: The Laker custom digital router